Scanning Microscopy Vol. 12, No. 1, 1998 (Pages 61-69) 0891-7035/98$5.00+.25
Scanning Microscopy International, Chicago (AMF O'Hare), IL 60666 USA

APPLICATION OF SCANNING TUNNELING/ATOMIC FORCE MICROSCOPE NANO-OXIDATION PROCESS TO ROOM TEMPERATURE OPERATED SINGLE ELECTRON TRANSISTOR AND OTHER DEVICES

Kazuhiko Matsumoto*

(Received for publication May 12, 1996, and in revised form February 8, 1997)

Abstract

Using a scanning tunneling microscope (STM) tip / atomic force microscope (AFM) cantilever as a cathode, the surface of titanium metal was oxidized to form a few tens of nanometers wide oxidized titanium line, which works as an energy barrier for the electron. Single electron transistors (SET), photoconductive switches, and high electron mobility transistors (HEMT) are fabricated using this process. The fabricated SET operates at room temperature showing the Coulomb gap and staircase with 160 mV periods, and the Coulomb oscillation with 400 mV periods. The fabricated photo-conductive switch shows a full width at half maximum (FWHM) response of 380 femtoseconds at a bias voltage of 10 V. The drain current of HEMT was controlled by the oxidized semiconductor wire on the channel region formed by this fabrication process.

Key Words: Scanning tunneling microscopy (STM), atomic force microscopy (AFM), nano- oxidation process, single electron transistor (SET), Coulomb gap, Coulomb staircase, Coulomb oscillation, Photoconductive switch, high electron mobility transistors (HEMT).

Electrotechnical Laboratory MITI, 1-1-4, Umezono,
Tsukuba-shi, Ibaraki-ken, 305, Japan
Telephone Number +81-298585516
FAX Number +81-298585523
E-mail:kmatumot@qm.etl.go.jp

Introduction

Recent nanostructure fabrication processes using scanning tunneling microscope (STM) and atomic force microscope (AFM) have undergone marked advances [1, 2, 5, 6, 9, 10] and are quite attractive for application to electron and optical devices. A few examples of such nanostructure fabrication process are as follows. Patterning and oxidation of the hydro passivated Si were demonstrated using the air ambient STM [1, 2], and a ~35 nm-wide line was obtained. Using the oxidized Si pattern as a mask, it was demonstrated that the Si substrate could be etched off down to 10 nm depth [9]. The thin titanium layer on the graphite substrate was oxidized and formed a ~20 nm-wide line by the anodization through the air-ambient water that existed between the STM tip and the titanium surface [10].

In this paper, we formed ultra fine oxidized titanium lines on the surface of a Ti layer on a SiO_2/Si substrate using the STM tip as a selective anodization electrode, and applied this nanometer-size oxidized titanium line to a single electron transistor [6, 7, 8]. A single electron transistor (SET) is considered to be a candidate for an element of a future low power, high density integrated circuit because of a possible ultra-low power operation with a few electrons. For practical applications, it is indispensable for the SET to be operated at room temperature. For this purpose, the size of the island of SET must be as small as ~10 nm to reduce the total capacitance of SET and to overcome the problems of the thermal fluctuation. However, the size of ~10 nm is out of the range of the present conventional microfabrication process. We present the fabrication of an SET using a new pattern formation method based on STM nano-oxidation process for the first time. The SET operates at room temperature, showing a clear Coulomb gap and staircase of ~160 mV period even at 300K. Ultrafast response of metal-semiconductor-metal photo-conductive switch has been realized by reducing the carrier lifetime by using low-temperature-grown substrates, or by fabricating narrow photoconductive gaps by electron beam lithography techniques. The fastest response yet, 0.87 ps, was achieved using a photoconductive switch with a 300 nm gap fabricated on a low-temperature-grown GaAs substrate. We fabricated a photoconductive switch by oxidizing a titanium thin film using an AFM [4]. In this paper, we report the fabrication

process and the characteristics of the switch. The response of the ultrafast switch was measured by an electron-optic (EO) sampling system. A full width at half maximum (FWHM) of 380 femtoseconds (fs) was obtained for the impulse response.

In order to control the current in the channel of a high-electron-mobility transistor (HEMT), normally they uses the metal gate on the channel region which can control the depth of the depletion layer by changing the gate bias. In this paper, semiconductor oxide wire on the channel region of the delta-doped HEMT was formed using the AFM, which can produce the depletion layer in the two-dimensional electron gas (2DEG) channel [3]. By changing the depth of the oxide wire, the current of the HEMT was controlled.

Nanometer Size Pattern Formation by STM/AFM

The pattern formation procedure by STM nano-oxidation process is shown in Figure 1. After deposition of the thin Ti layer (3 nm thick) at the low pressure of 10^{-7} Torr, the sample was set in an air ambient STM. The Ti surface was biased positively to the Pt STM tip. When the STM tip is posistioned near the Ti surface, not only the tunneling current but also the Faraday current flow between the tip and the surface through the water, which is in the atmosphere. Then the Ti surface was oxidized to form titanium oxide (TiOx). By scanning the STM tip, fine TiOx lines were formed. When the bias polarity was inverted, no pattern was formed at all, which indicates that the pattern was formed electrochemically. Figure 2 shows the three oxidized Ti lines on the Ti surface formed by STM, using a sample bias Vt (tunneling voltage) of 5 V, a sample current It (tunneling current) of 1 nA, and a scanning speed of 0.01 mm/sec. The line-width and height are 80 nm and 4 nm, respectively.

The pattern made by the STM process was analyzed by micro-Auger analysis, and the obtained result is shown in Figure 3. Before this micro-Auger analysis, the native oxide of the Ti surface, which was spontaneously oxidized by the ambient air, was completely sputtered off. In Figure 3, a clear peak of the oxygen at the kinetic energy of ~500 eV can be observed, as well as a Ti peak. The distribution of the oxygen in the sample was also checked by micro-Auger analysis, and only from the pattern made by the STM process, a large amount of oxygen was detected. From these two results of the micro-Auger analysis, we may conclude that the STM process oxidized the Ti surface.

The dependence of the line size on the scanning speed of the STM tip is shown in Figure 4. By increasing the scanning speed from 0.01 μm/sec to 3 μm/sec at Vt = 5 V, It = 1 nA, the line width and the line height decrease drastically from 45 nm to 18 nm, and from 3.5 nm to 2.5 nm, respectively. This result indicates that by increasing the scanning speed of the STM tip the Faraday current that flows between the tip and the Ti surface per unit length decreases. Therefore, the formed oxidized Ti line width and height decrease.

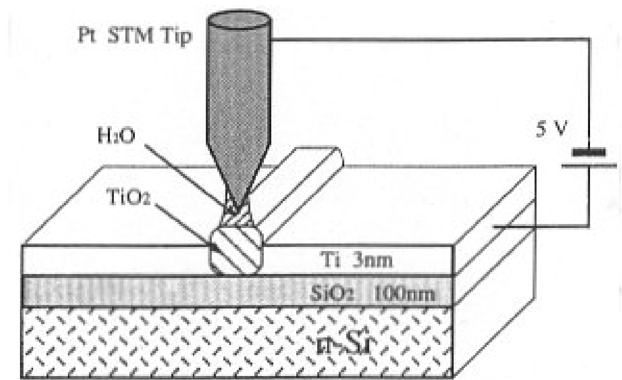

Figure 1. Principle of Ti oxidation process using STM tip as anodization electrode. Substrate is SiO_2/Si.

Single Electron Transistors with Different Structures

Using the above mentioned STM nano-oxidation process, two types of single electron transistors (SET) were fabricated. The main differences of the type of SET are: (1) the position of the gate electrode, and (2) the number of the tunneling junctions, i.e., the number of the islands of the SET. Figure 5 shows the schematic illustration of the SET with the gate electrode on the back side of the n-Si substrate. At both ends of the 3 nm thick Ti layer, the source and drain Ohmic contacts are formed by depositing Ti/Au pad metal. At the center region of the Ti layer, the island region is formed which is surrounded by the two parallel narrow TiOx lines that will work as tunneling junctions for the SET and the two large TiOx barrier regions which works as an insulator between the source and drain. These TiOx lines and the large TiOx barrier regions are made by the STM nano-oxidation process. Figure 6 shows a three dimensional view by AFM of the island region of the fabricated SET. Two narrow TiOx lines which work as tunneling junctions are seen between two large TiOx barrier regions. The island is surrounded by those TiOx lines and barriers.

The typical size of the TiOx line is 15-20 nm wide and 30-50 nm long. The island size is 20-30 nm by 30-50 nm. The most important feature of this structure is that the tunnel junction area that corresponds to the cross-section of the TiOx line is as small as 2-3 nm (the thickness of the Ti layer) by 30-50 nm (the length of the TiOx line). The deposited Ti layer is as thin as 3 nm, and the surface of the Ti layer is spontaneously oxidized about 1 nm. Therefore, the intrinsic Ti layer thickness is considered to be less than 3 nm. Owing

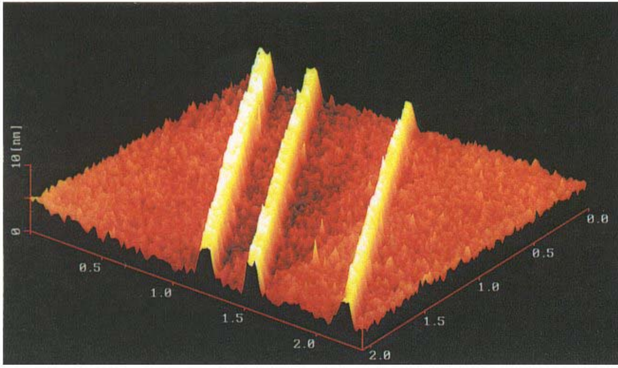

Figure 2. Three oxidized Ti lines formed by STM anodization method. Line width is 80 nm, line height is 4 nm. Scanning speed of 0.01 mm/sec, sample bias Vt = 5V, sample current It = 1 nA.

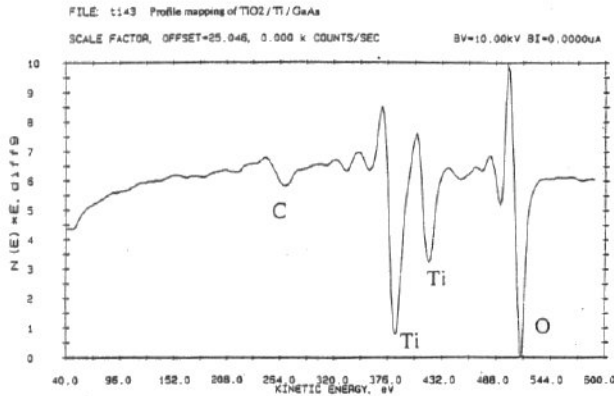

Figure 3. Micro-Auger analysis of pattern made by STM process. Clear peak of oxygen was detected as well as Ti peak and carbon peak.

to this small tunneling junction area, the tunnel capacitance becomes as small as the order of 10^{-19} F, which makes it possible to operate the SET at room temperature as will be shown in the following.

Figure 7 shows the schematic illustration of the SET with the side gate electrode structure. The structure has one island between the source and drain regions. The gate electrode is separated from the island region by a 500 nm wide oxidized TiOx region which can completely suppress the gate leak current to the drain current and works as the gate insulator. By increasing the number of tunneling junctions, the multi-island structure is easily fabricated. Figure 8 shows the plain view of the AFM image of the fabricated side gate SET with three tunneling junctions, i.e., two islands SET. Figure 9 shows

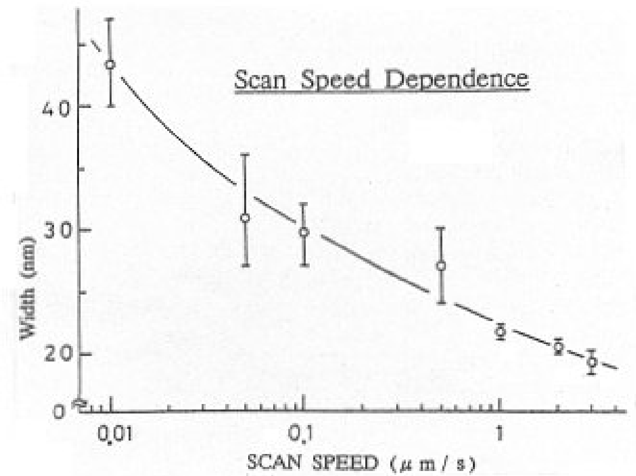

Figure 4. Dependence of oxidized Ti line width on scanning speed of STM tip. Sample bias Vt = 5 V. Sample current It = 1 nA.

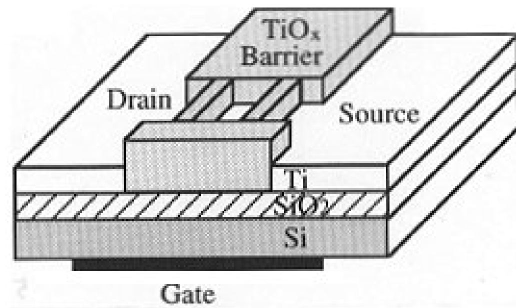

Figure 5. Schematic illustration of back gate SET made by STM nano-oxidation process.

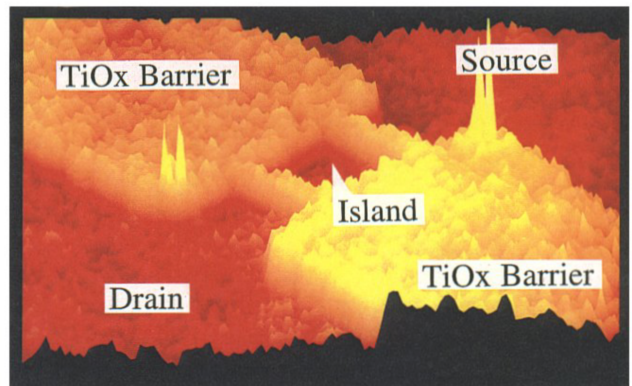

Figure 6. Three-dimensional AFM image of fabricated back gate SET with one island structure.

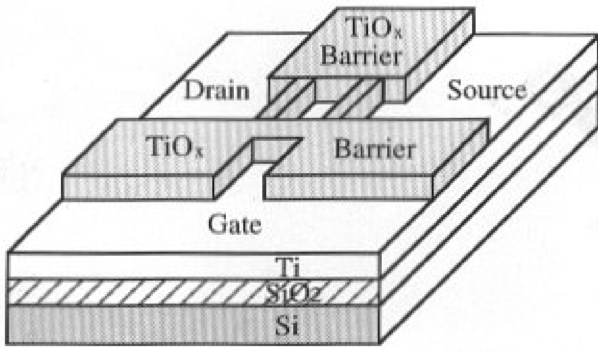

Figure 7. Schematic illustration of side gate SET made by STM nano-oxidation process.

---

the measured size of the three tunneling junctions and two islands of the side gate SET of Figure 8 by AFM. From Figure 9, the tunneling junction size of 15 nm wide and the island size of 28 nm wide are obtained.

Figure 10 shows the drain current-drain voltage characteristics of the side gate SET with 5 islands structure at room temperature with the gate terminal kept open. The clear Coulomb gap of about 160 mV is seen at around zero drain voltage. There is no leak current seen in the Coulomb gap. This may be attributed to the multi-tunneling junctions which can drastically decrease the co-tunneling current. The Coulomb staircases with almost the same periodicity are also obtained even at room temperature. The first Coulomb staircase at +180 mV and -180 mV are clearly seen.

The gate bias dependence of the drain current of the side gate SET with three tunneling junctions and two island structure was examined at room temperature and is shown in Figure 11. The drain bias was set at V_D = 10 mV and the gate bias was changed from 0 V to -5 V. The four large oscillations of the current were seen at around the gate voltage (V_G) = -2.7 V, -3.1 V, -3.5 V, -3.9 V and these current oscillations have a strict periodicity of 400 mV. Therefore, it could be concluded that this current oscillation was the Coulomb oscillation. From this periodicity of the Coulomb oscillation, the gate capacitance (Cg) of the side gate SET was calculated to be Cg = 0.4 aF. The reason why there are no Coulomb oscillations observed between the gate bias of Vg = 0 V and -3.6 V is not clear.

Photoconductive Switch

In this section, the fabrication process and the characteristics of the photoconductive switch will be shown. The response of the ultrafast switch was measured by an electro-optic (EO) sampling system.

The electro-optical switch was fabricated on the Ti layer which was deposited on the semi-insulating GaAs substrate. Using the STM nano-oxidation process, the titanium layer was completely oxidized, which was confirmed by the high resistance (10 MΩ) across the gap of 100 nm TiOx wire. The length of the oxide wire was 5 µm, the same as the width of the conductors of a transmission line. Breakdown did not occur in the photoconductive switch until the bias voltage reached 11 V. It is possible that the insulator prevents breakdown along the semiconductor surface or through the air gap between the electrodes.

This oxide wire is not only transparent to the excitation beam but also a good insulator. After oxidation, a coplanar transmission line were formed with a gap on the sample. The metal conductors were made of Ti/Au and were 5 µm wide and 200 nm thick. The line separation was 5 µm. The distance between the thick conductors of the bias line and the signal line was 5 µm. We removed the titanium thin film except for the part constituting the photoconductive switch by reactive ion etching. The fabrication process of the switch is shown in Figure 12.

The response of this photoconductive switch was measured using an EO sampling system incorporating a colliding pulse mode-locked (CPM) dye laser (Fig. 13). The laser provided a 40 femtoseconds (fs) optical pulse train (= 620 nm) at a repetition rate of 94.2 MHz. The average output power was 10 mW, and the laser beam was divided into an excitation beam for the switching and a probe beam for measurement. The device under test is shown in Figure 14. The probe beam passes through the probe crystal and is reflected at its bottom surface by a dielectric mirror deposited on the probe crystal. The probe crystal is made of 50-µm thick $LiTaO_3$, the x axis of which is perpendicular to the surface of the sample. This configuration is sensitive to the vector component of the electric field along both the y axis and the z axis. The sensitivity to a vector component of the electric field along the y axis is proportional to the electro-optic coefficient τ_{22} (1 pm/V) and the sensitivity to a vector component of electric field along the z axis is proportional to the coefficient (τ_{33} - τ_{13}) (27.9 pm/V). We set the z axis of the probe crystal parallel to the transverse electric field. The longitudinal component of the electric field is negligible in this case because the coefficient τ_{22} is small compared to (τ_{33} - τ_{13}). The output signal is considered to be the transverse component of the electric field. The probe beam passing through a compensator is decomposed into two polarized components which are detected by two slow Si photodetectors. The electrical output signal is measured through a lock-in amplifier. The time resolution of the system is determined by the optical pulse width (40 fs), the spot size (< 5 µm) of the sampling beam and the probe configuration. It takes about 50 fs for the electrical signal to pass through the laser spot. The time resolution is also determined by the transit time of optical pulses passing through the probe crystal,

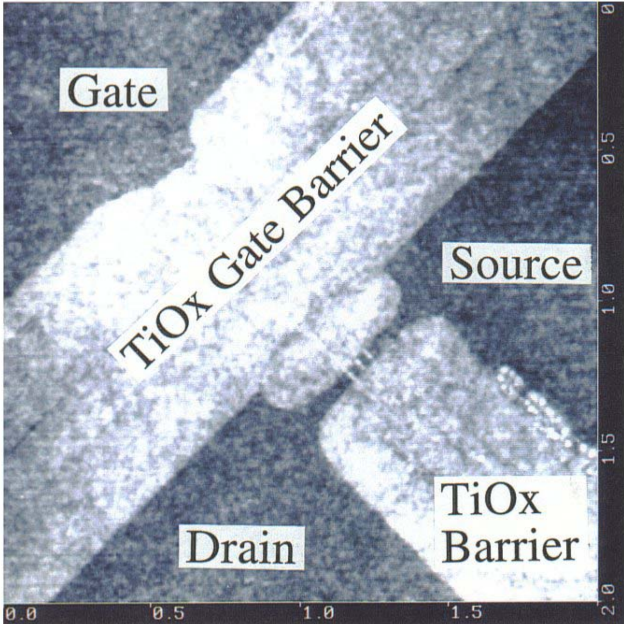

Figure 8. Plain view of AFM image of fabricated side gate SET with two islands structure.

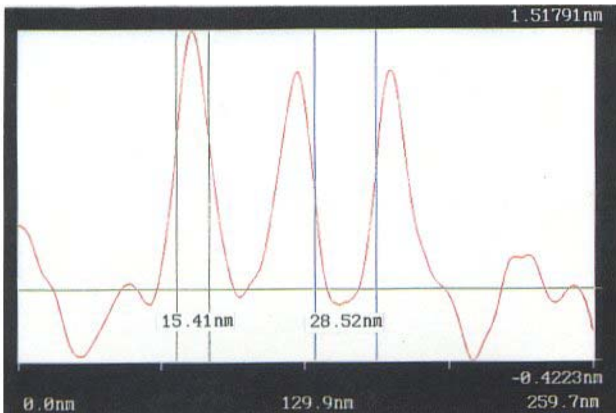

Figure 9. Size of tunneling junction and island of two islands SET measured by AFM.

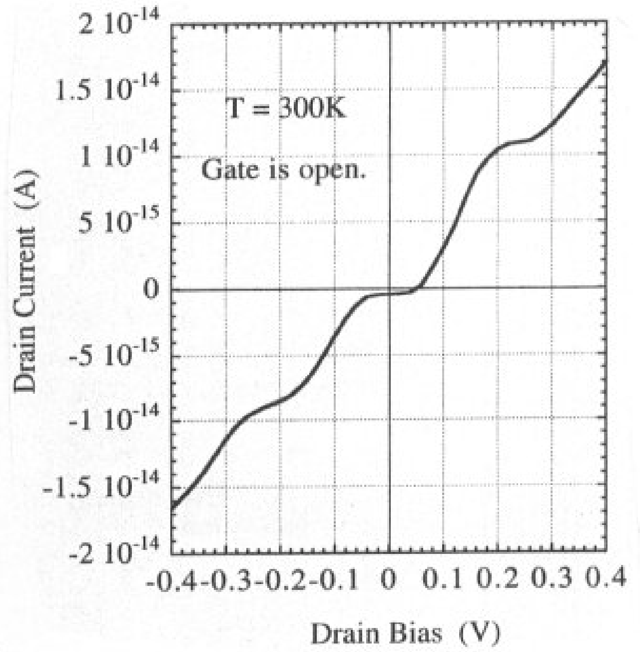

Figure 10. Drain current-voltage characteristics of side gate SET with 5 islands structure at room temperature with gate terminal kept open. Clear Coulomb gap and staircases with 160 mV periods are seen.

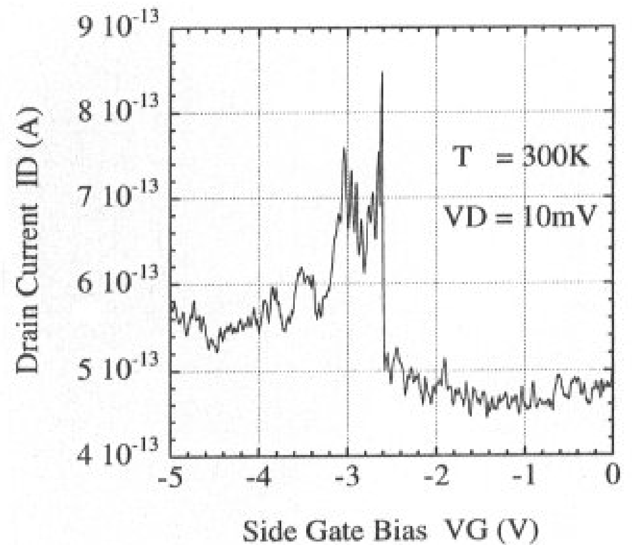

Figure 11. Gate bias dependence of drain current of side gate SET with two island structure at room temperature. Drain bias was set at VD = 10 mV. Coulomb oscillation with periods of 400 mV are seen at VG = -2.7 V, -3.1 V, -3.5 V, and -3.9 V.

---

and the spatial distribution of the electric field in the probe. The transit time through the probe is calculated as 730 fs from the thickness (50 μm) of the probe. The spatial distribution of the electric field depends on the configuration of the probe and the device being tested. The electric field in the crystal is not uniform and is influenced by the dielectric mirror. The time resolution of the whole system is estimated to be less than 200 fs from the measured 10-90% rise time for the photoconductive switch.

The impulse response for the ultrafast

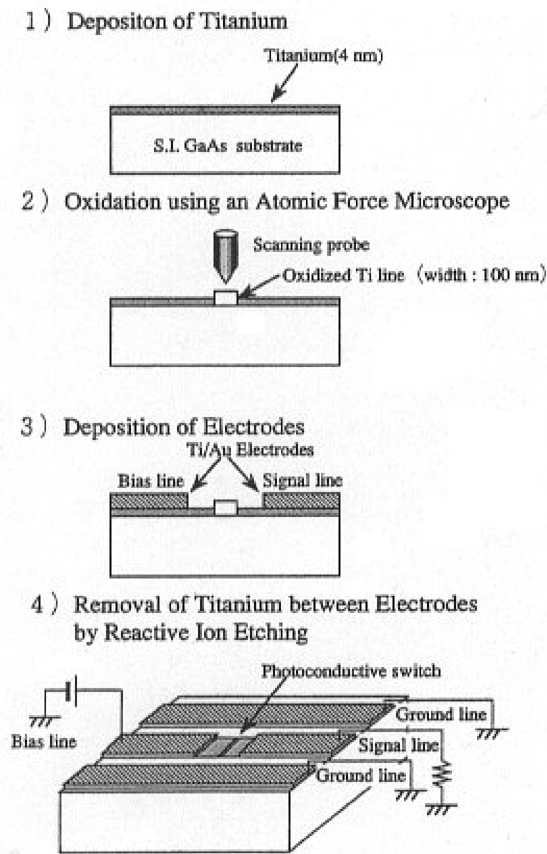

Figure 12. Fabrication process of photoconductive switch.

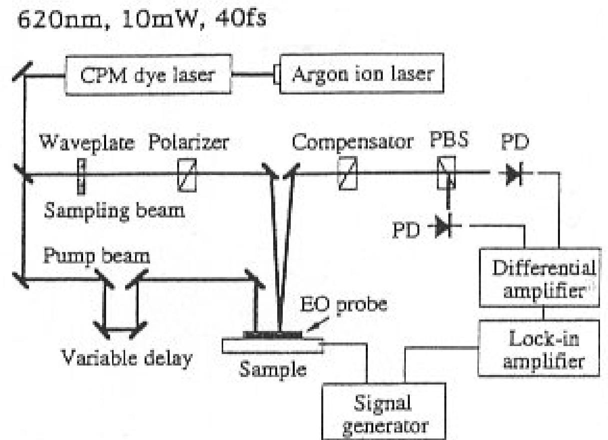

Figure 13. Electro-optic sampling system incorporating a colliding pulse mode-locked dye laser.

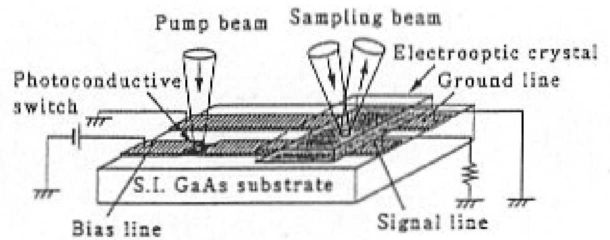

Figure 14. Configuration of external electro-optic probe and device under test.

photoconductive switch is shown in Figure 15. A FWHM response time of 380 fs was obtained 80 μm away from the photoconductive gap at a bias voltage of 10 V. The electric field at the semiconductor surface was 10^3 kV/cm.

The transit time through the photoconductive gap is calculated from the saturation velocity as 1.2 ps (8.3 x 10^6 m/s, 100 nm) for electrons and 2.0 ps (5.0 x 10^6 m/s, 100 nm) for holes. These values are much larger than the measured pulse width. The photo-excited electrons reach a maximum velocity of around 10^8 cm/s in 100 fs. This value is calculated using a simple Monte Carlo simulation based on the model without considering the screening effect of the photo-excited carriers. This means that the photo-excited electrons move about 50 nm in 100 fs. This phenomenon, which is known as velocity overshoot, explains the measured fast response of the switch. The measured electrical pulses are broadened at the sampling point by the resistance and capacitance (RC) charging time for the switch and the transmission line. The capacitance of the oxidized titanium is calculated to be 8.5 aF (1 aF = 10^{-18} F) from the measured dielectric constant ($\varepsilon_r = 24$), which is much smaller than the capacitance of the GaAs substrate. The slow decay after the electron current due to the velocity overshoot, includes the hole current and probably the electron current photo-excited deep inside the substrate.

The peak intensity of the signal corresponds to the transverse electric field at the static voltage of 4 V, and is almost half of the bias voltage. The peak intensity is equal to half of the bias voltage for an ideal photoconductive switch. This means that the conductance is changed dramatically by the excitation beam.

Current Control of High Electron Mobility Transistor (HEMT)

Using the conductive AFM cantilever coated with Au, not only the metal surface, but also the semiconductor surface could be oxidized to form the oxidized semiconductor wire illustrated in Figure 16. The oxidized semiconductor wire forms the depletion layer inside the semiconductor, which controls the drain current in the HEMT.

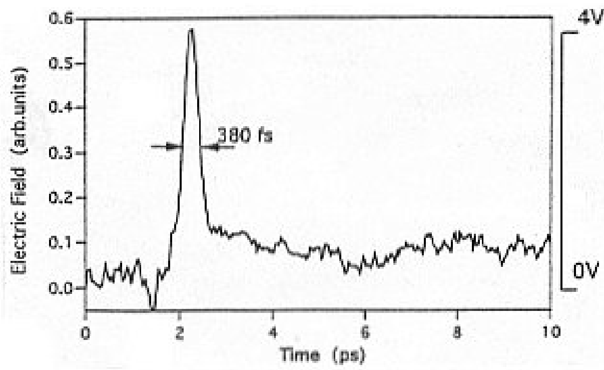

Figure 15. Out put signal from photoconductive switch measured using electro-optic sampling system.

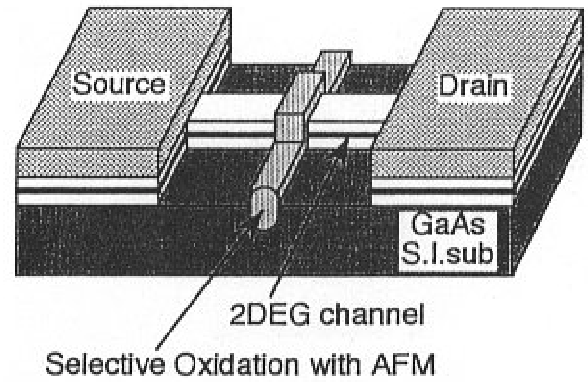

Figure 17. Fabricated delta-doped HEMT structure with semiconductor oxide wire on channel region.

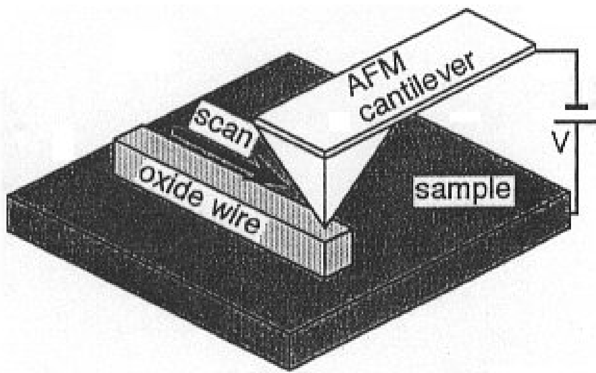

Figure 16. Selective oxidation procedure using AFM for semiconductor surface.

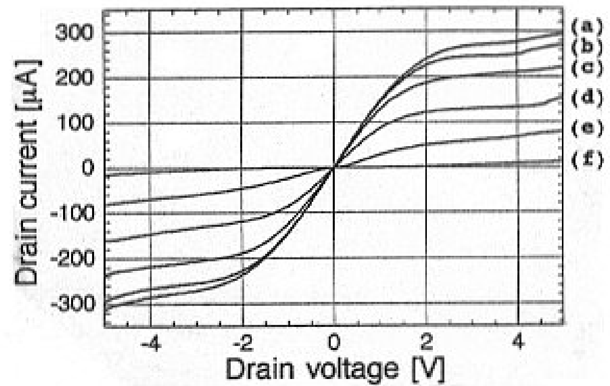

Figure 18. Current-voltage characteristics of delta-doped HEMT with semiconductor oxide wire. Wire height are (**a**) no oxide wire, (**b**) 3 nm, (**c**) 10 nm, (**d**) 12 nm, (**e**) 17 nm, and (**f**) 20 nm.

The fabricated HEMT structure is shown in Figure 17. To investigate whether the oxide wire actually produces the depletion layer or not, the oxide wire was formed on the channel region. The sample is the delta-doped HEMT structure grown by molecular-beam-epitaxy (MBE) method. The epitaxial layer consists of undoped AlGaAs (20 nm thick), a delta-doped Si layer (5×10^{13} cm^{-2}), undoped AlGaAs (4 nm) and undoped GaAs (500 nm) on a semi-insulating GaAs substrate. The 2DEG channel region was fabricated by chemical etching. The channel width and length are 1 μm and 7 μm, respectively. The source and drain ohmic contacts were formed on both sides of the channel.

The oxidation process was performed across the channel to control the drain current. An oxide wire was formed at the scanning speed of 10 nm/s. The applied bias between the AFM cantilever and the semiconductor was changed from 10 V to 25 V to change the depth of the oxide wire in the channel, that is, the depth of the depletion layer. If the depletion layer is produced by the oxide wire, the drain current of HEMT should be decreased.

The current-voltage characteristics of HEMT with the oxide wire are shown in Figure 18. The height of the oxide wire was controlled by changing the applied voltage. The height of the wire increased with applied voltage. We considered that the depth of the oxide wire also increased proportional to the height of the wire. Before the formation of the oxide wire, we confirmed that almost the same characteristics were observed for all samples. The drain current decreased as the height of the wire increased as shown in Figure 18. With the oxide wire of 20 nm height formed at 25 V, the current was approximately a hundred times lower than that of the samples without the wire. The decrease of the current in Figure 18

shows that the oxide wire produces the depletion layer in the 2DEG channel. Moreover, Figure 18 shows that the depth of the depletion layers could be controlled through the wire height.

Conclusion

We were the first to successfully apply the STM/-AFM nano-oxidation process to a single electron transistor. The SET operated at room temperature. The SET shows the Coulomb gap and staircase of about 160 mV periods and Coulomb oscillation of 400 mV periods at room temperature. The Coulomb gap, staircase and Coulomb oscillations observed at room temperature are attributed to the small tunneling junction area made by the STM/AFM nano-oxidation process.

An ultrafast photoconductive switch with a gap of 100 nm was fabricated using the STM/AFM nano-oxidation process. The fast response of the switch is not explained by the saturation velocity of photo-excited carriers, but it can be explained by the velocity overshoot phenomenon. A FWHM impulse response of 380 fs is obtained for a bias voltage of 10 V. These are the fastest photoconductive switches of their kinds so far fabricated, to our knowledge.

The current of the HEMT was controlled by the oxide wire formed by the AFM. By changing the height of the oxide wire, i.e., by changing the depth of the depletion layer, the drain current of the HEMT was easily controlled by monitoring the height of the oxide wire. This process could be applied to the more complicated quantum effect devices based on the 2-dimensional electron gas system.

The STM/AFM nano-oxidation process is quite easy and could be applicable to any kind of devices. We open a new frontier for new nanometer size device processes.

References

[1] Dagata JA, Schneir J, Harary HH, Evans CJ, Postek MT, Bennett J (1990) Modification of hydrogen-passivated silicon by a scanning tunneling microscope operating in air. Appl. Phys. Lett. **56**, 2001-2003.

[2] Dagata JA, Schneir J, Harary HH, Bennett J, Tseng W (1991) Pattern generation on semiconductor surface by a scanning tunneling microscope operating in air. J. Vac. Sci. Technol. **B9**, 1384-1388.

[3] Ishii M, Matsumoto K (1995) Control of current in 2DEG channel by oxide wire formed using AFM. Jpn. J. Appl. Phys. **34**, 1329-1331.

[4] Itatani T, Segawa K, Matsumoto K, Ishii M, Nakagawa Y, Sugiyama Y, Oota K (1995) 380 fs electrical pulse generation from 100nm insulator - gap photoconductive switches fabricated by an Atomic Force Microscope. In: Extended Abstracts of the International Conference on Solid State Devices and Materials, Osaka. Japan Society of Applied Physics, Tokyo. pp. 980-982 (abstract).

[5] Lyding JW, Shen TC, Hubacek JS, Tucker JR, Abeln GC (1994) Nanoscale patterning and oxidation of H-passivated Si(100)-2x1 surface with an ultrahigh vaccum scanning tunneling microscope. Appl. Phys. Lett. **64**, 2010-2012.

[6] Matsumoto K, Takahashi S, Ishii M, Hoshi M, Kurokawa A, Ichimura S, Ando A (1995) Application of STM nanometer size oxidation process to planar-type MIM diode. Jpn. J. Appl. Phys. **34**, 1387-1390.

[7] Matsumoto K, Ishii M, Shirakashi J, Segawa K, Oka Y, Vartanian BJ, Hariss JS (1995) Comparison of experimental and theoretical results of room temperature operated single electron transistor made by STM/AFM nano-oxidation process. Technical Digest of International Electron Device Meeting. Electron Device Society, IEEE, New York. pp. 363-366.

[8] Matsumoto K, Ishii M, Segawa K, Oka Y, Vartanian BJ, Hariss JS (1996) Room temperature operation of a single electron transistor made by the scanning tunneling microscope nanooxidation process for the TiOx/Ti system. Appl. Phys. Lett. **68**, 34-36.

[9] Snow ES, Campbell PM (1994) Fabrication of Si nanostructure with an atomic force microscope. Appl. Phys. Lett. **64**, 1932-1934.

[10] Sugimura H, Uchida T, Kitamura N, Masuhara H (1993) Nanofabrication of titanium surface by tip-induced anodization in Scanning Tunneling Microscopy. Jpn. J. Appl. Phys. **32**, L553-L555.

Discussion with Reviewers

H. Iwasaki: Formation of the depletion layer or the accumulation layer inside the semiconductor by oxidation would depend on the type of the semiconductor and details such as how interface states and fixed charges in the oxide film are formed and the oxide surface is charged. The experimental result given in **Current Control of High Electron Mobility Transistor (HEMT)** indicates that the depletion layer is formed in your case. How do you interpret this result?
Author: In the current controll of HEMT, the depletion layer is formed just under the oxide semiconducotor owing to the interface states and the fixed charges in it. The details of the mechanism how these interface states and the fixed charges are related to the formation of the depletion is not clear now.

P.M. Campbell: Your devices operate in the range of fractions of a picoampere, which will limit their range of applications. How can you raise the current to a more practical level? Have you tried thicker films (say up to 10 mm)?
Author: We did not try to use thicker films up to 10 nm because the oxidation does not reach the bottom. In order to increase the current of the SET, the thickness of the tunneling junctions

should be decreased, or in other words, the oxide wire should be made narrower. For this purpose, the humidity of the ambient atmosphere of the STM should be controlled more precisely.